Analog/mixed-signal education and design with open-source models, processes, and PDKs

Chipshub Faculty Fellows Train the Trainers Workshop
Design Automation Conference,
Long Beach, CA -- 2026-07-22

Slides at the top of https://lab.davidburnett.org

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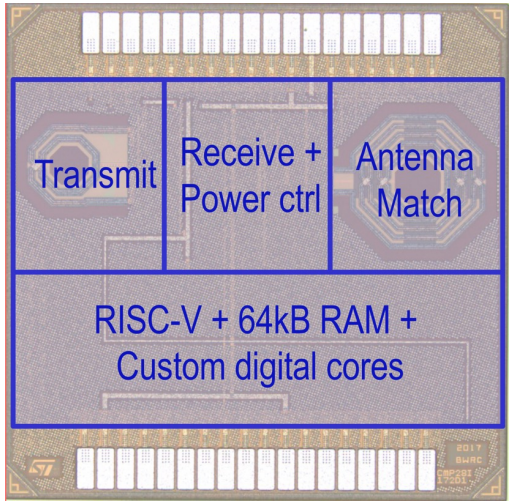
VILLANOVA ENGINEERING

My background: RF SoC tapeout classes at UC Berkeley (ST 28), Portland State U (Intel 16), Villanova U (TBD)

Created, taught "impossible" new tapeout class in 2017
Millions of $$ invested since!



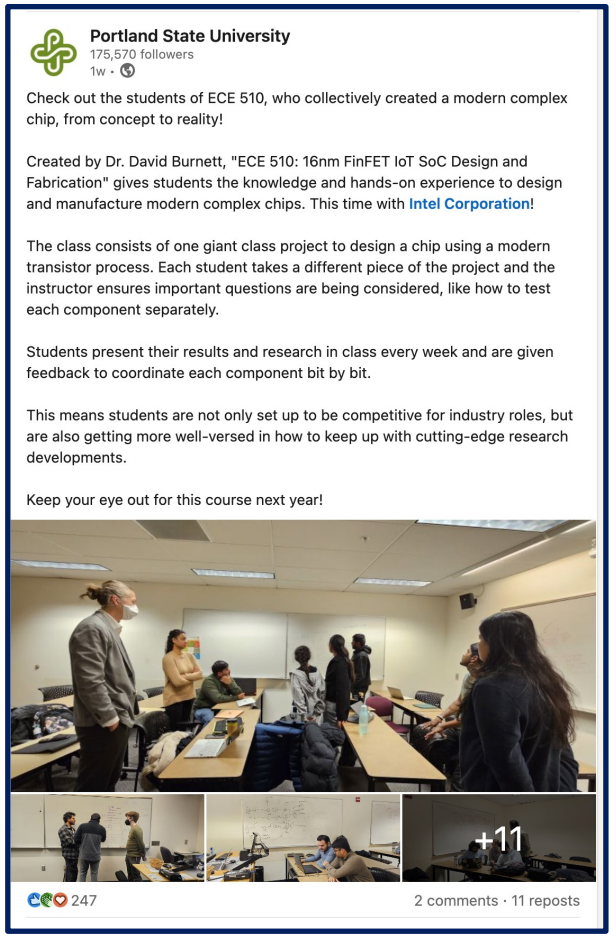
2.4 GHz BLE TxRx
32-bit RISC-V CPU

1.1 mm x 1.1 mm
ST 28 FD-SOI

D. C. Burnett, B. Kilberg, R. Zoll, O. Khan, and K. S. J. Pister, "Tapeout class: Taking students from schematic to silicon in one semester," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1–5, doi: 10.1109/ISCAS.2018.8351506.

Preparing dice for students, jewelry for faculty

Tapeout Class '17 reunion



Intel Mindshare Curriculum funding +
Intel University Shuttle Program 16 nm FinFET

Why I got involved in Chipshub: the fastest way to expand American chip design

- Learning IC design at University of Washington and UC Berkeley? Easy to take the infrastructure for granted!
  - All thanks to Lee Damon and Brian Richards, respectively
- Building the infrastructure for IC design teaching and research? A multi-year hassle! Big barrier to starting IC design at new schools
  - 💸 Spec, buy, install my own server (oh, it takes three months to ship…)
  - 👨‍💻 Linux setup, or: try it again with **`sudo`**
  - ❌ University admin: no way, NDA!
  - 🔐 DIY data security and access control policies
  - 🪳 Pipecleaning: Gosh, this PDK requires really specific tool versions
  - 🤝 Hello, my name is Prof. Sysadmin

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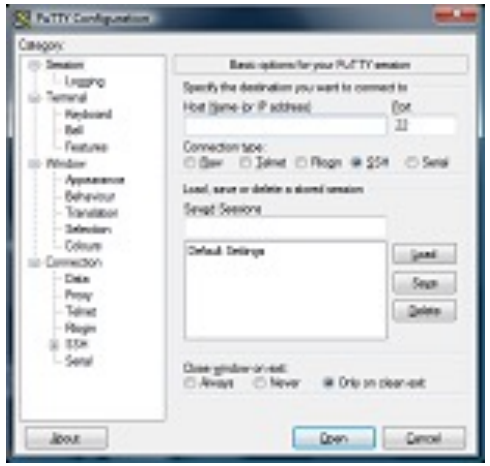
How do you and your students run Virtuoso?

Making a connection

- PuTTY
- SSH
- VNC
- X windows
- WSL
- RDP
- NoMachine, NICE DCV, x2go, RustDesk…



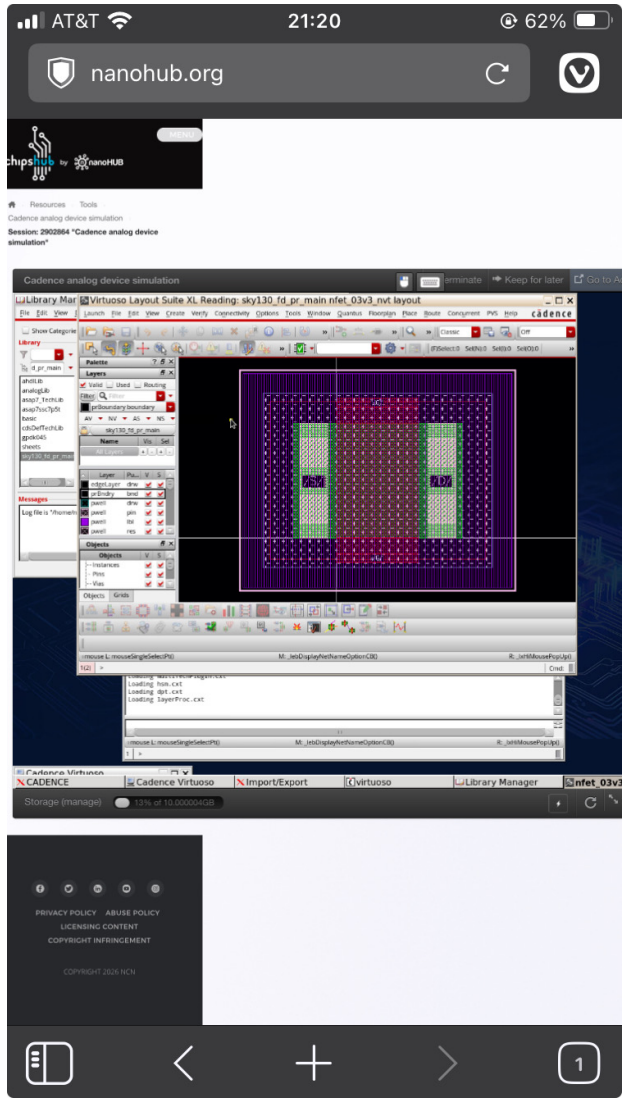
putty.org

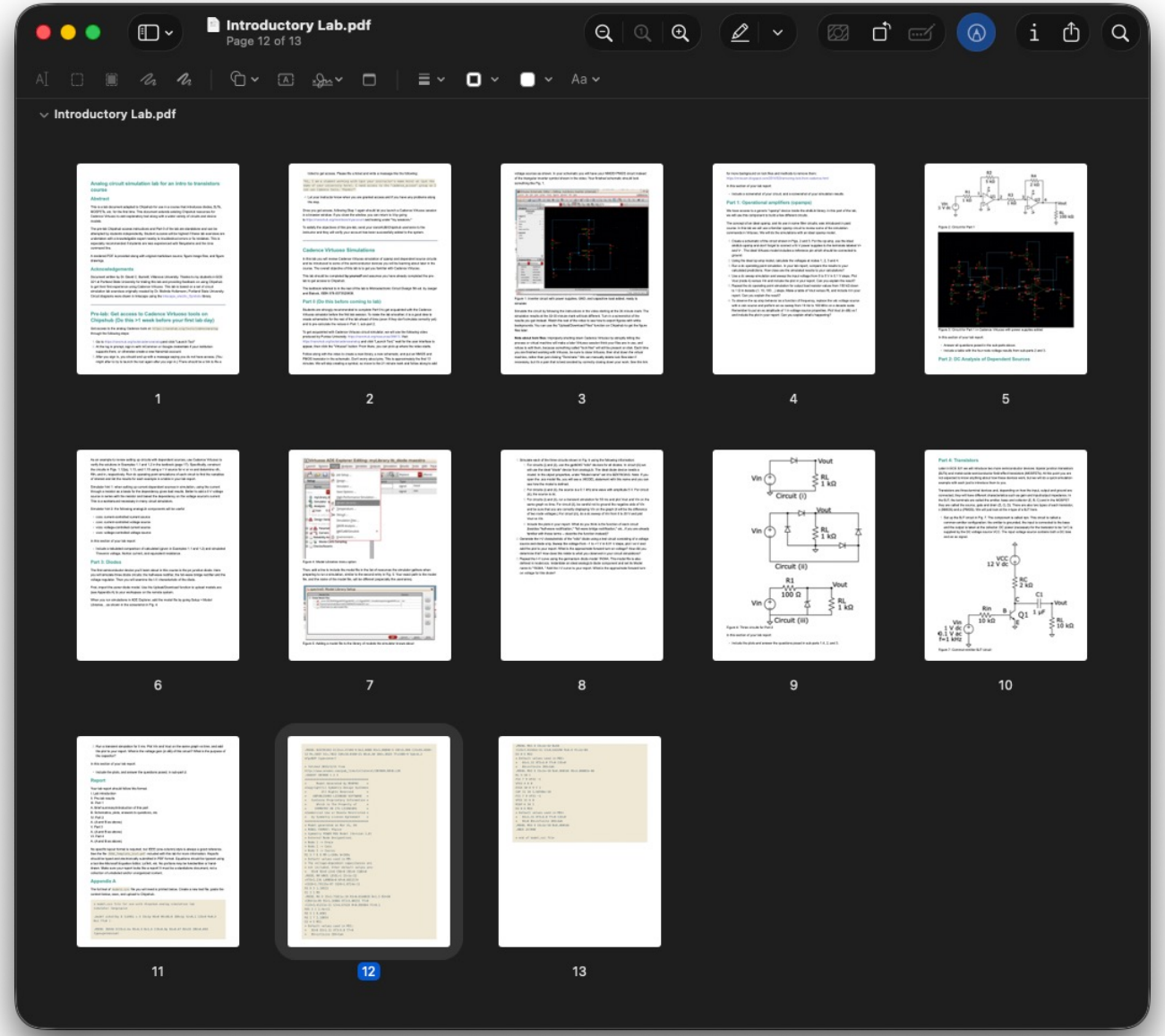
Trying to use Linux for the first time

- `virtuoso&`
- "`scp` your files to…"
- "`cd`"?
- "untar the archive…"
- "I closed my laptop and all my work is gone!"
- "VNC asking for a password?"

1 "Getting-started" lab for analog simulation

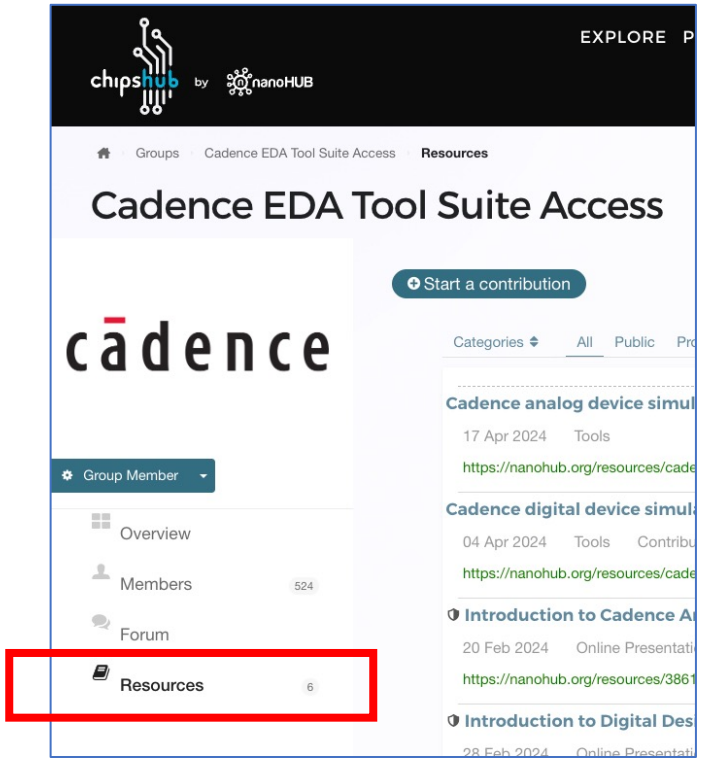
- Make it as easy as LTspice!
  - Two+ weeks of the term often spent on the "how" of working on a remote server. Skip all that with Chipshub
  - Teach using professional-grade software, easily
- Things we needed to iron out during the testflight term:
  - Students kill sessions! Lab document says not to but…
    - Auto-clear some log files; if Virtuoso sees 10 log files it won't start
  - Added better text editors and support for many terminals
    - IC design has more command line work and gluing of tools together
  - Class-wide library files: work with staff to host on server
  - TBA: Long sims and overnight sessions may be "cleaned up"





Should appear soon with the cadence_access group under "Resources"

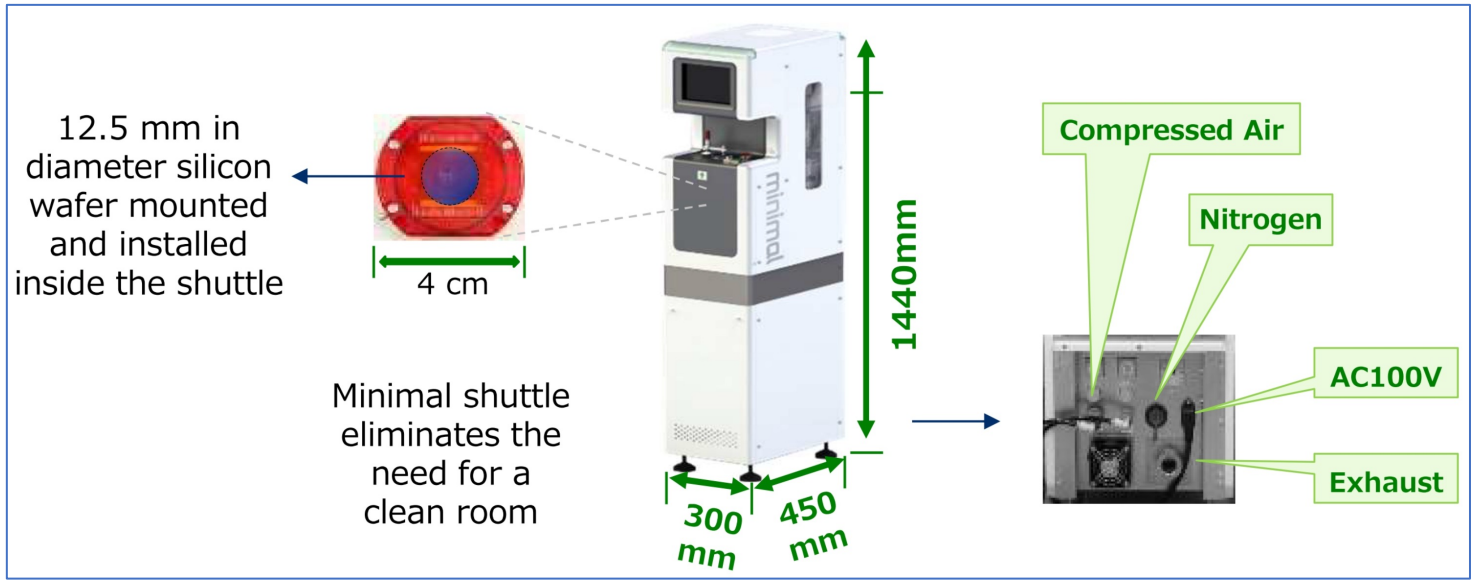
https://nanohub.org/groups/cadence_access/resources



2 Fast CMOS+X Tapeout Class: Yokogawa Minimal Fab PDK on Chipshub

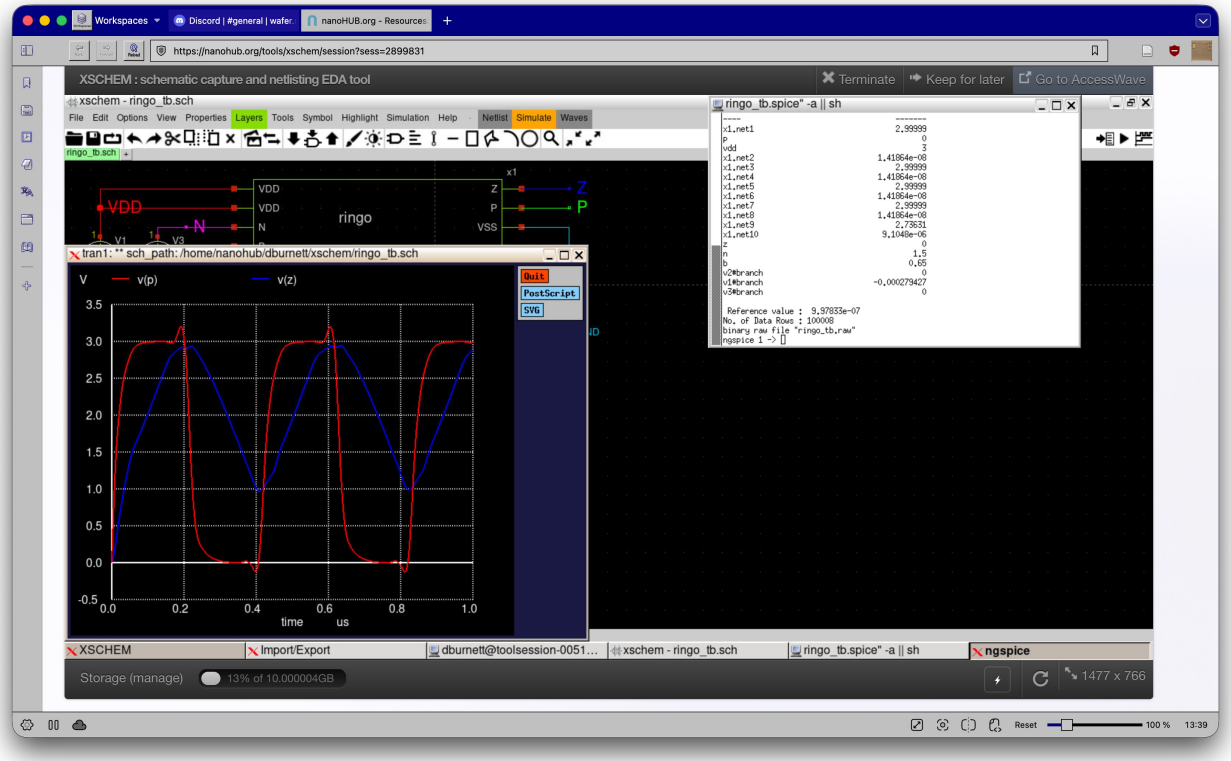
- Cleanroom-in-an-office using sealed 12 mm wafers
- ~1 week turnaround -- ultrafast CMOS+X (and more) prototyping
- 1 µm CMOS PDK established for open-source toolchain

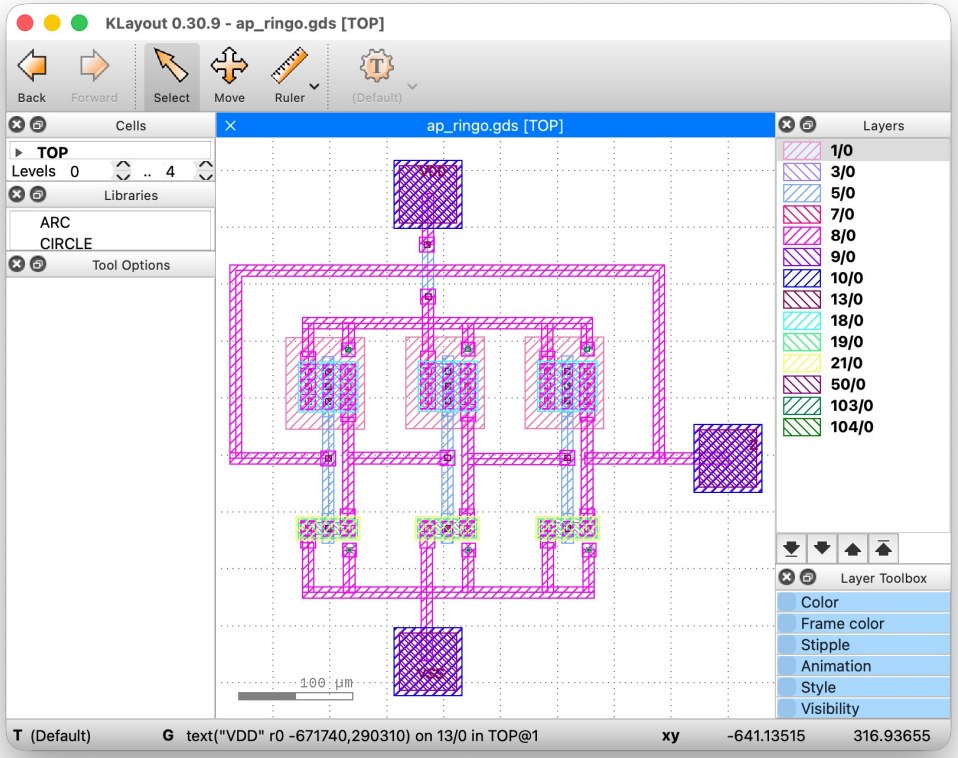
yokogawa.com



yokogawa.com

- Goal: eliminate the tapeout class fab bottleneck!
- Current status: ongoing undergraduate research project to demonstrate proof of concept
  - No MPW program yet; joining shuttle run some time next year





Designs by Andrew Parra, undergraduate researcher in the Burnett Lab at Villanova University

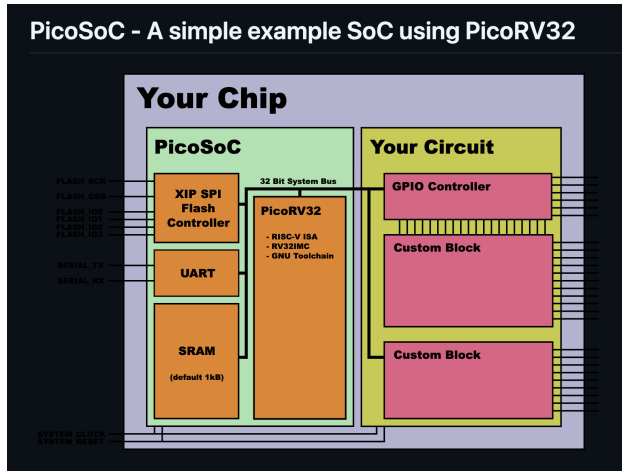
3 Tapeout class groundwork with PicoRV32 and the wafer.space MPW service

wafer.space

Google + GLOBAL FOUNDRIES

FOSS 180nm Production PDK
github.com/google/gf180mcu-pdk

LibreLane



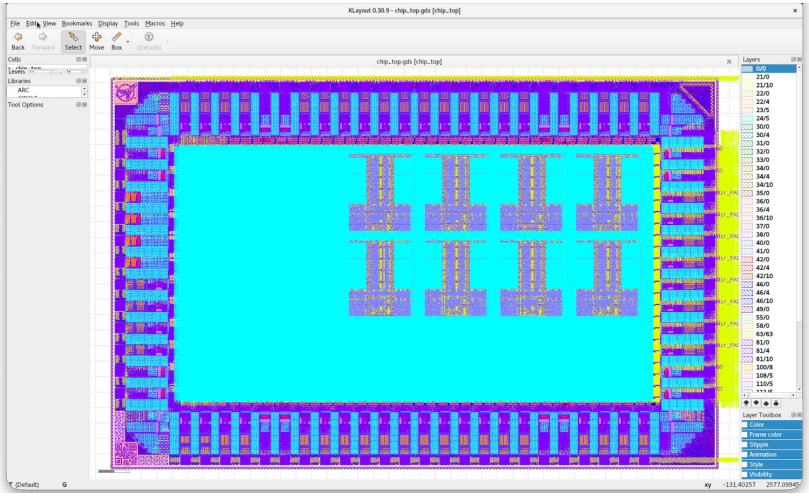
https://github.com/YosysHQ/picorv32/tree/main/picosoc

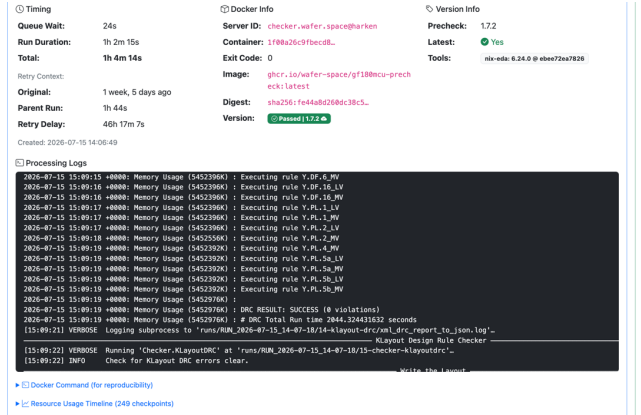
- Open-source GF180MCU design aggregator, 1000 pcs returned
  - Bare dice "quarter slot" (~4 mm^2) for $3,000; full wafers for $2,000 ea
- LibreLane (new OpenLane) toolchain most well-supported
- Yosys has released PicoRV32 CPU, PicoSoC, Lattice FPGA project
- Can we use these parts to find an cheap, simple path to silicon?

I put together a PicoSoC-based ASIC, made the GDS on Chipshub and shipped it to wafer.space

https://github.com/burnettlab/picosoc-on-waferspace

- Transition from FPGA to ASIC can be tough!
  - Lots of FPGA PicoSoC material out there. Need a min. viable example for ASIC.
- New Chipshub tool created: "Librelane (high memory)" w/ 32 GB RAM
  - Librelane config.yaml must be edited to limit threads to 16
  - Processes get SIGKILL if they try to grab too much RAM ☹

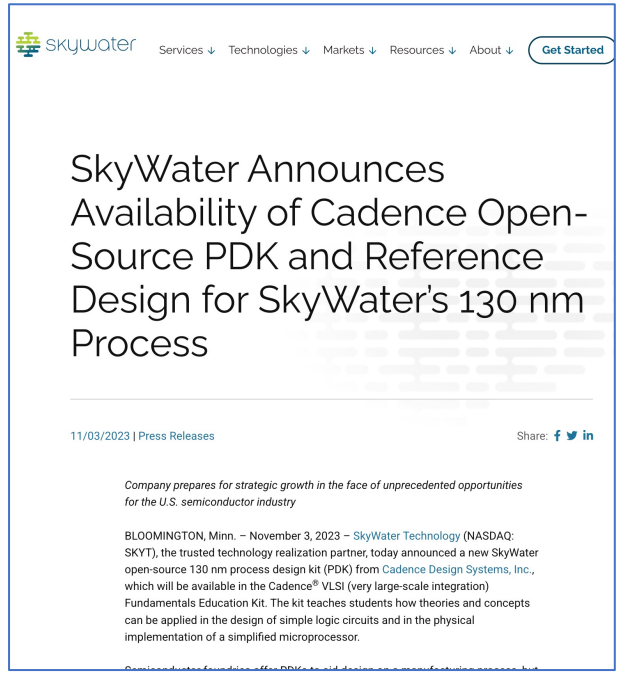




Ready for manufacturing!

My Chipshub roadmap

- Cadence + SKY130 FOSS PDK
  - Best of both worlds for training: commercial-grade tools with manufacturable PDK needing no NDA
  - Familiarizing with manufacturable process → faster undergraduate research contributions… if SKY130 lives on
- gm/id lookup table design in python
  - Pre-compute the tables and put them on Chipshub!
  - See Brandon Hippe's poster here at DAC on Mon and Tue!
- More SoC design tools: SiliconCompiler, VACASK…
- Faster design of SoCs to support novel circuits!

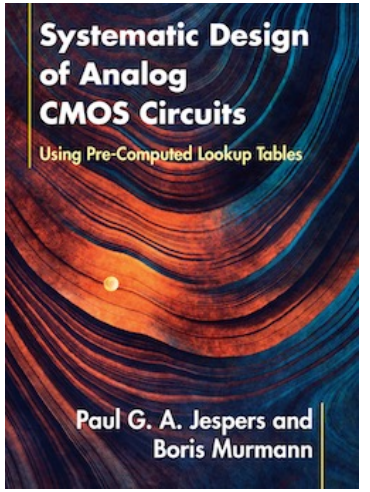

skywater Services Technologies Markets Resources About Get Started

SkyWater Announces Availability of Cadence Open-Source PDK and Reference Design for SkyWater's 130 nm Process

11/03/2023 | Press Releases Share:

Company prepares for strategic growth in the face of unprecedented opportunities for the U.S. semiconductor industry

BLOOMINGTON, Minn. – November 3, 2023 – SkyWater Technology (NASDAQ: SKYT), the trusted technology realization partner, today announced a new SkyWater open-source 130 nm process design kit (PDK) from Cadence Design Systems, Inc., which will be available in the Cadence® VLSI (very large-scale integration) Fundamentals Education Kit. The kit teaches students how theories and concepts can be applied in the design of simple logic circuits and in the physical implementation of a simplified microprocessor.



https://github.com/bmurmann/Book-on-gm-ID-design

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